

WHAT IS CLAIMED IS:

1. An electro-optical panel driving circuit, comprising:
 - a substrate;
 - pixel electrodes provided above the substrate;
 - switching elements that switch on and off the corresponding pixel electrodes;
 - data lines that supply image signals to the corresponding pixel electrodes via the corresponding switching elements;
 - a shift register circuit that sequentially outputs transfer signals;
 - a buffer circuit that buffers the sequentially output transfer signals;
 - a sampling circuit that samples the image signals using the buffered transfer signals as sampling pulses and that supplies the sampled image signals to the corresponding data lines; and
 - a dummy circuit that simulates at least part of the buffer circuit and the sampling circuit,
delay signals indicating the amount of delay of the sampling pulses and generated by the dummy circuit being fed back to the shift register circuit so that the amount of delay is reduced, and
 - the buffer circuit, the sampling circuit, and the dummy circuit provided on the substrate.
2. The electro-optical panel driving circuit according to Claim 1, the shift register circuit provided in an integrated circuit externally attached to the substrate.
3. The electro-optical panel driving circuit according to Claim 1, the buffer circuit including a plurality of stages of buffers connected in series,
 - the sampling circuit including analog sampling switches, and
 - the dummy circuit simulates at least the buffer in the final stage among the plurality of stages of buffers.
4. The electro-optical panel driving circuit according to Claim 3, the dummy circuit simulates the sampling switches and all of the plurality of stages of buffers.
5. The electro-optical panel driving circuit according to Claim 1, semiconductor elements constituting the sampling circuit formed in the same process and at the same time as semiconductor elements constituting the corresponding dummy circuit.
6. The electro-optical panel driving circuit according to Claim 5, each of the semiconductor elements is an N-type semiconductor element.

7. The electro-optical panel driving circuit according to Claim 5, further comprising:

a timing adjusting circuit, each of the semiconductor elements being a thin-film transistor,

the source of the thin-film transistor connected to a low-potential power supply of the driving circuit and the drain of the thin-film transistor biased at a high-potential power supply of the driving circuit and connected to a detection terminal of the driving circuit,

the shift register circuit sequentially outputting the transfer signals in accordance with a clock cycle of clock signals, and

the timing adjusting circuit adjusting the timing of the clock signals input to the shift register circuit on the basis of the timing of the falling edge of the delay signals detected by the detection terminal.

8. The electro-optical panel driving circuit according to Claim 1, further comprising:

a timing adjusting circuit,

the shift register circuit sequentially outputting the transfer signals in accordance with a clock cycle of clock signals, and

the timing adjusting circuit adjusting the timing of the clock signals input to the shift register circuit on the basis of the amount of delay indicated by the delay signals.

9. The electro-optical panel driving circuit according to Claim 8, the shift register circuit and the timing adjusting circuit provided in an integrated circuit externally attached to the substrate.

10. The electro-optical panel driving circuit according to Claim 1, the channel width of first thin-film transistors constituting the sampling circuit equal to the channel width of second thin-film transistors constituting the dummy circuit, the second thin-film transistors corresponding to the first thin-film transistors.

11. The electro-optical panel driving circuit according to Claim 1, the channel width of second thin-film transistors constituting the dummy circuit, the second thin-film transistors corresponding to first thin-film transistors constituting the sampling circuit, being smaller than or equal to the channel width of the first thin-film transistors, and

the ratio of the size of the first thin-film transistors to the size of a first buffer circuit in the preceding stage of the first thin-film transistors being equal to the ratio of the size of the second thin-film transistors of the dummy circuit to the size of a second buffer circuit in the preceding stage of the second thin-film transistors.

12. The electro-optical panel driving circuit according to Claim 1, the buffer circuit including a plurality of stages of buffers connected in series,
the sampling circuit including analog sampling switches,
the channel width of second thin-film transistors constituting the dummy circuit, the second thin-film transistors corresponding to first thin-film transistors functioning as the sampling switches, being smaller than or equal to the channel width of the first thin-film transistors, and
the ratio of the size of the first thin-film transistors to the size of the buffer in the final stage of the first buffer circuit in the preceding stage of the first thin-film transistors being equal to the ratio of the size of the second thin-film transistors of the dummy circuit to the size of the buffer in the final stage of a second buffer circuit in the preceding stage of the second thin-film transistors.

13. An electro-optical device comprising the electro-optical panel driving circuit as set forth in Claim 1 and the electro-optical panel driven by the driving circuit.

14. An electronic apparatus, comprising:
the electro-optical device as set forth in Claim 13.